REMARKS

The Applicants appreciate the thoroughness with which the subject application has been examined and the allowance of claims 23-41. By this amendment, changes have been made in claims 1, 20, 23, 42 and 43 to overcome the Examiner's rejections and objections and more concisely claim and describe the present invention. Claims 1-45 remain in the application for reconsideration by the Examiner. The Examiner's allowance of all pending claims is earnestly solicited.

MATTERS RELATED TO THE SPECIFICATION

The patent application referred to as the parent of the instant application has issued, and accordingly the Applicants have revised the reference in the specification to include the issued patent number.

The Examiner has objected to the specification, stating that the terms "offset spacers" as recited in claims 11 and 38 are not expressly mentioned in the specification.

To overcome this rejection, the Applicants have amended the references to layers 211 and 216, as shown in Figure 1B to include a reference to an offset spacer. See the specification amendments set forth above. These layers can function as the offset spacers and thus support the objected to claim language.

MATTERS RELATED TO THE CLAIMS

The Examiner has rejected claims 1-22 and 42-44 under Section 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicants regard as the invention. In particular, the Examiner states that "silicon plug" in claim 1 lacks antecedent basis.

The Applicants have amended the claim as set forth above, replacing "silicon plug" with "semiconductor plug," which is referred to elsewhere in claim 1. Thus the rejection of claims 1-19 is believed to be overcome as "semiconductor plug" has a proper antecedent basis in the claim 1.

As to claims 20, 22, 42 and 44, the Examiner suggests certain discrepancies between elements set forth in these dependent claims and the independent claims from which they depend.

The Examiner is invited to review the marked-up version of claim 20 wherein the Applicants have added a further step of, "forming a gate electrode adjacent the gate . . ." to overcome the rejection. The gate is referred to in claim 1, "forming a gate in contact with the semiconductor plug, wherein the gate is of a second conductivity type." Thus the material types set forth in claim 20 now relate to the gate electrode. It is believed that this amendment to claim 20 should overcome the rejection of that claim under Section 112, second paragraph. The Examiner is invited to review the paragraphs beginning at line 24 on page 11 (wherein the MOSFET gate electrode is discussed) and the two successive paragraphs beginning at line 8 on page 12 (wherein the JFET gate electrode and its relationship to the MOSFET gate electrode is discussed), which support these amendments.

Claim 21 has been revised for consistency with the language of claim 20 from which it depends. Claim 22, also depending from claim 20, remains as originally submitted. Both these claims should also now satisfy the requirements of Section 112, second paragraph.

As to the rejection of claim 42, the Applicants have amended the claim as set forth above to refer to, "a gate electrode material," and have also amended independent claim 23 from which claim 42 depends to refer to, "a gate electrode." The material types set forth in claim 42 now refer to materials of the gate electrode. Claim 43 depends from claim 42 and has been amended for consistency with the amendment to claim 42. Claim 44 dependent from claim 42 remains as originally submitted. Support for these claim amendments can be found in the same specification paragraphs as cited above relative to the rejection of claims 20-22. Given these amendments, the rejection of claims 42, 43 and 44 under Section 112, second paragraph, is believed to have been overcome.

The Examiner has rejected claims 1-22 under Section 103(a) as unpatentable over Hergenrother (6,027,975) taken with Choi (4,700,461) and Miyazawa (5,312,782).

As to the rejection of independent claim 1, it is noted that there is no disclosure or suggestion in Hergenrother, Choi, or Miyazawa that permits their combination as suggested by the Examiner. In particular, it is noted that the process of Hergenrother discloses, "forming a

window in the at least three layers of material," "filling the window with a semiconductor material," "removing the second layer," (a sacrificial layer), "forming a layer of dielectric material on the exposed portion of the semiconductor plug," and "forming a gate in contact with the layer of dielectric material." Miyazawa illustrates in Figure 11 a "vertical channel field effect transistor [that] includes no gate insulating film and a semiconductor layer 111 thereof [which] must be of the n- type reverse to that of a polycrystalline silicon 119 as a gate electrode on the outer side." Since Miyazawa lacks any disclosure of the various Hergenrother steps, including those set forth above, there can be no basis for combining Hergenrother and Miyazawa to disclose the Applicants' invention. The structure of Miyazawa cannot be made by the process of Hergenrother; the process of Hergenrother cannot be used to fabricate the structure of Miyazawa. Absent a suggestion to combine Hergenrother and Miyazawa, there is no reason why one skilled in the art, with no prior knowledge of the Applicant's invention, would make that combination when faced with the problem confronting the Applicants. The only suggestion for combining Hergenrother and Miyazawa to arrive at the claimed invention stems from hindsight knowledge derived from the Applicant's invention. The two references simply are not combinable with reference to the Applicants' process of fabricating a vertical transistor as set forth in independent claim 1.

As to Choi, he discloses a lateral junction-field effect transistor and is not combinable with Hergenrother or Miyazawa, both of which disclose vertical transistors. Choi is not combinable with Hergenrother, as the steps disclosed in Hergenrother for forming a MOSFET disclose forming a vertical MOSFET, whereas Choi's disclosure relates to a planar or linear MOSFET wherein the various doped regions are fabricated in a horizontal configuration.

Thus it is respectfully requested that claim 1 as amended is patentably distinct from the cited prior art.

With respect to the rejection of claims 2-22 under Section 103(a), it is respectfully submitted that dependent claims 2-22, depending either directly or indirectly from independent claim 1 are in condition for allowance. Each of these dependent claims further distinguishes the invention over the art of record as each includes one or more elements in conjunction with the elements of claim 1 that are not present in the art of record.

Claim 45, related to fabricating matched junction field effect transistors, has been rejected under Section 103(a) as unpatentable over Hergenrother taken with Choi and Miyazawa, as applied to claims 1-22 and further in view of Fitch (5,414,289).

While Fitch discloses a vertical transistor, Fitch does not describe the various Hergenrother steps of "forming a window in the at least three layers of material," "filling the window with a semiconductor material," "removing the second layer," (a sacrificial layer), "forming a layer of dielectric material on the exposed portion of the semiconductor plug," and "forming a gate in contact with the layer of dielectric material." Fitch cannot be combinable with Hergenrother since Fitch discloses a different technique for forming a vertical transistor. Fitch forms, "a sidewall dielectric . . . laterally adjacent the control electrode [gate] conductive layer. The conductive layer at least partially surrounds a channel region. A vertical conductive region is formed within a device opening." Further, Fitch discloses regions of different conductivities formed within the window of Figure 1.

Given the dissimilar processes disclosed by Hergenrother and Fitch (and Miyazawa as described above), it is respectfully submitted that these references are not combinable in accordance with relevant doctrines of reference combinability. It is therefore suggested that claim 45 is allowable over the prior art of record. The fact that it would be desirable, according to the Examiner, "to form a plurality of matched junction field effect transistors at the same time so as to reduce production costs and time", does not satisfy the requirements for permitting the combination of the references. A desirable result does not satisfy the requirement that there must be some suggestion or inference in at least one of the references as to how it would be combined with another cited reference.

Given the inability to combine the references cited against claim 45, it is respectfully submitted that this claim is in allowable condition.

The Applicants have attempted to comply with all of the points raised in the Office Action and it is believed that the remaining claims in the application, i.e., claims 1-45, are now in condition for allowance. In view of the foregoing amendments and discussion, it is requested that the Examiner's claim rejections have been overcome. It is respectfully requested that the Examiner reconsider these rejections and objections and issue a Notice of Allowance for all the claims pending in the application.

The Applicants hereby petition for an extension of time of one month to February 1, 2005 under the provisions of 37 C.F.R. 1.136. An Authorization to Charge Credit Card Account for the $120 extension fee is enclosed.

If a telephone conference will assist in clarifying or expediting this Amendment or the claim changes made herein, the Examiner is invited to contact the undersigned at the telephone number below.

Respectfully submitted,

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CERTIFICATE OF MAILING

I HEREBY CERTIFY that this Amendment is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 1st day of February, 2005.

John L. DeAngelis, Jr.